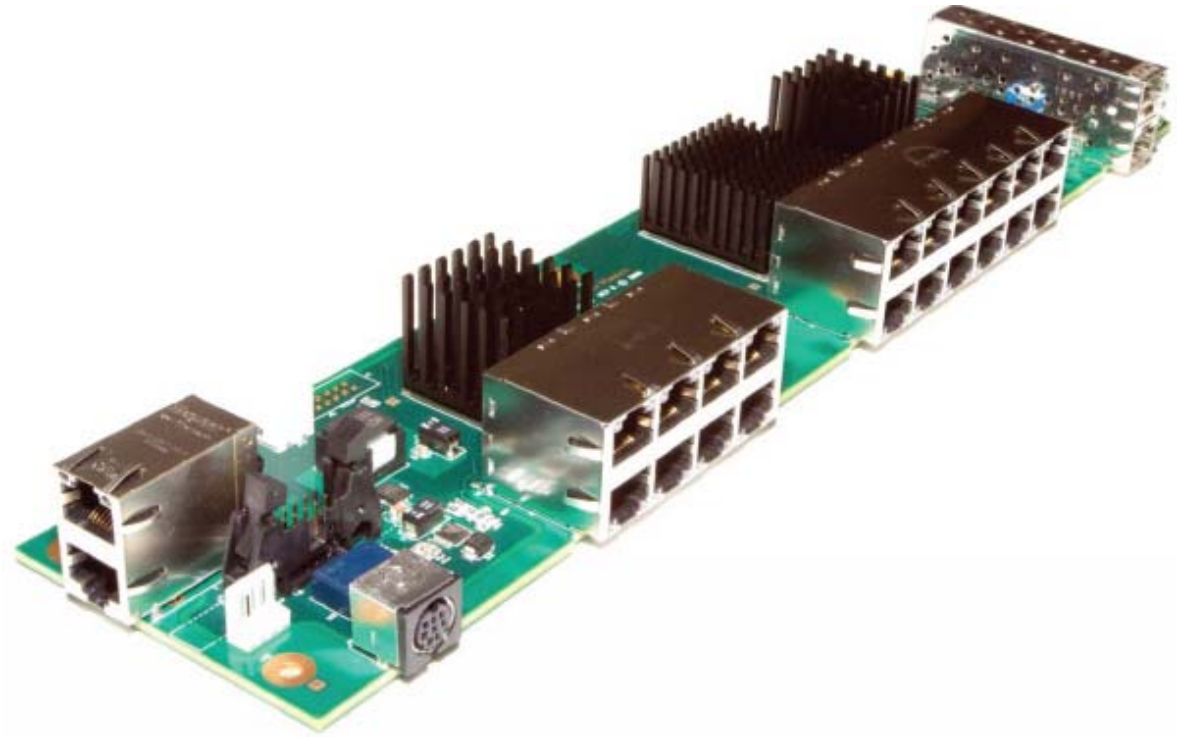
Interface Masters
TECHNOLOGIES
Innovative Network Solutions

Niagara 1301
User Guide



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1. Overview

Niagara 130x is a new generations of 100/1000Mbps Embedded Switches (ES) products targeted to networking appliances, servers, server blades and embedded computing applications. The Niagara 130x Family is a fully featured embedded Ethernet switch that provides Layer2 Gigabit Ethernet and is ready to be integrated into servers by connecting via a serial or Ethernet connection. The family is based on the Vitesse SparX-G24 and provides no blocking, wire-speed Gigabit performance on all ports, using an internal 46-Gbps frame bus. The devices are optimized for SMB and SOHO for unmanaged, as well as managed, applications.

1.1 Feature Summary

- General Features
  - Support twenty 1000BASE-T, and two Fiber SFP Switching
  - Provide USB Utility Interface.
  - Software support for, Linux 2.4.x, and FreeBSD 7.x
  - IEEE 802.3ab, 802.3z, 802.3u, 802.3x compliant
  - Gigabit Ethernet ports with no blocking wire-speed performance
  - 8,192 MAC addresses and 4,096 VALN support (IEEE std 802.1Q)
  - 8,192 IP multicast groups supported
  - Jumbo Frame support at all speeds (10/100/1000) of up to 10 Kilobytes
- Layer 2 Switching
  - Rapid Spanning Tree Protocol support (IEEE Std 802.1w)
  - Multiple Spanning Tree support (IEEE Std 802.1s)
  - IGMP, GARP, GMRP, and GVRP support
- Quality of Service
  - Programmable multi-layer classifier with four QoS classes per port
  - Strict priority or weighted round-robin forwarding with guaranteed bandwidth allocation
  - Traffic class assignment based on port, 802.1p tag, or Diffserve Code Point (DSCP) field
  - DSCP (IPv4 and IPv6) and IEEE Std 802,1o support
  - DSCP remarking for both IPv4 and IPv6 packets
  - Provider Bridging support with multiple VLAN tags (Q-in-Q)
  - Broadcast and multicast storm control
  - Full duplex flow control (IEEE Std 802.3x) and half duplex back pressure
  - Traffic shaping and policing per port in steps of 128kbps
  - Link aggregation support based on Layer 2-4 information (IEEE Std 802.3ad)

- Security
  - Port-based access control support (IEEE Std 802,1X)
  - 4096 VLAN support (IEEE Std 802.1Q)
  - VLAN awareness on a per port basis
  - Independent and shared VLAN learning
  - VLAN Q-in-Q support (VLAN stacking)
  - Source IP filter per port to block unwanted access
  - Extensive snooping: BPDU, GARP, ARP, IPMC, IGMP, TCP/UDP
  - TCP/UDP filter for CPU copy/redirect, frame snooping and frame eradication
  - DHCP filter to block unwanted DHCP servers on a per-port basis
  - Multiple ARP filters for detection of ARP intrusion scans
  - Extensive storm control: broadcast, multicast, unicast, ICMP and CPU (ARP, BPDU)
  - Per port CPU based learning option
  - CPU mirroring per port and per VLAN

1.2 Mechanical Specification

Dimension

The dimension for Niagara 1301 is 12.99” x 2.96” (324.75mm x 74.12mm), L x H.

Weight

The weight for Niagara 1301 is xx oz.

1.3 Environmental Specification

The Niagara 1301 is designed to operate under following conditions

Temperature

Operating 0°C to 70°
Storage -30°C to +70°

Relative Humidity

TBA

Altitude

TBA

Vibration tolerance

15 Gs on 3 axes

Physical shock

30 Gs on 3 axes

1.4 Input Power Requirement

Niagara 1301 draws the required power from the Motherboard Power Supply. Niagara1301 requires +1.2V, +5V and +3.3V to operate correctly.

	Voltages				Unit
	1.2	3.3	5		Volt
Total Current Per Voltage	7500	3100	TBD		mA
Total Power per voltage	9	10.23	TBD		Watt
Total Power	19.23				Watt
Total Raw power	20				Watt

Table 1, Power Requirement

2. Hardware Interface

Niagara 1301 has the following interfaces as indicated in Figure1 and Figure 2:

Gigabit Ethernet Switch Interface:

- Twenty four 100/1000 BASE-T Gigabit Ethernet Ports.
- Two Fiber SFP Ports.
- Two 100/1000BASE-T Internal Gigabit Ethernet Ports.

Other Interface:

- Dual Power Supply Sockets
- USB interface
- Serial Console Port
- Dip Switch
- 5V Power Supply Port
- 5V power Supply Port for LED panel
- Link/Activity Indicating LEDS

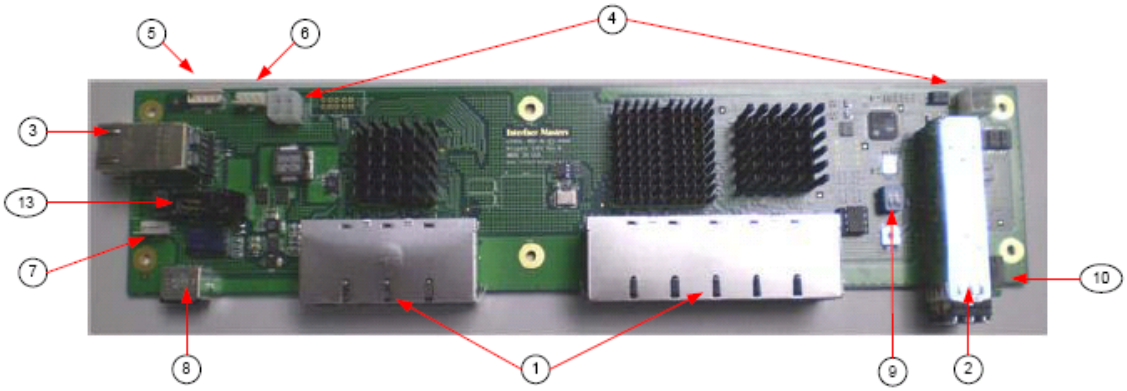

Figure 1, Top View of Niagara 1301.

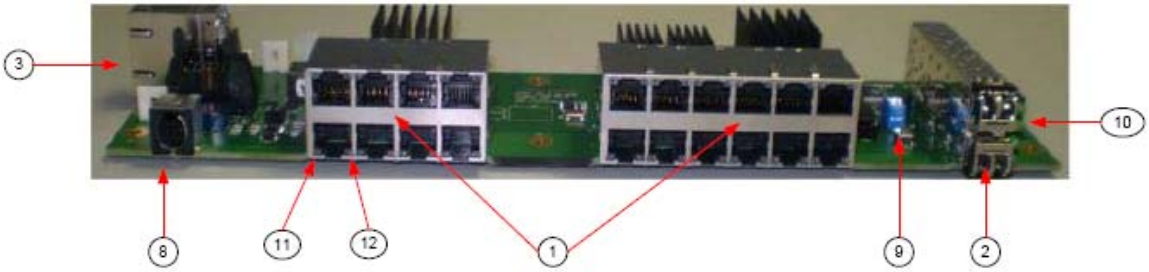

Figure 2, Front View of Niagara 1301.

1. 20 100/1000 BASE-T Gigabit Ethernet Ports.
2. 2 Fiber SFP Pots for 1000BASE-LX or 1000BASE-SX
3. 2 100/1000 BASE-T Internal Gigabit Ethernet Ports
4. Dual Power Supply input sockets for 5V and 3.3V
5. USB interface
6. 5V Power Supply output
7. 5V Power Supply output for LED panel
8. Serial Console interface input
9. Dip Switch
10. Link/Activity LED (Green) for 2 1000BASE-LX or 1000BASE-SX Ports
11. Activity LED (Green) for 1000BASE-T Port
12. Link LED (Orange) for 1000BASE-T Port
13. Serial Console interface output

2.1 Theory of Operation

Niagara 1301 is preconfigured as a un-managed Gigabit Switch.

Two internal Gigabit Ethernet Ports can be connected with the Ethernet Port on the motherboard.

Twenty front Gigabit Ethernet Ports can be connected to any 100/1000BASE-T appliance.

Two Fiber SFP sockets can be plug in with 1000BASE-LX or 1000BASE-SX SFP modules to be connected with 1000BASE-LX or 1000BASE-SX appliance.

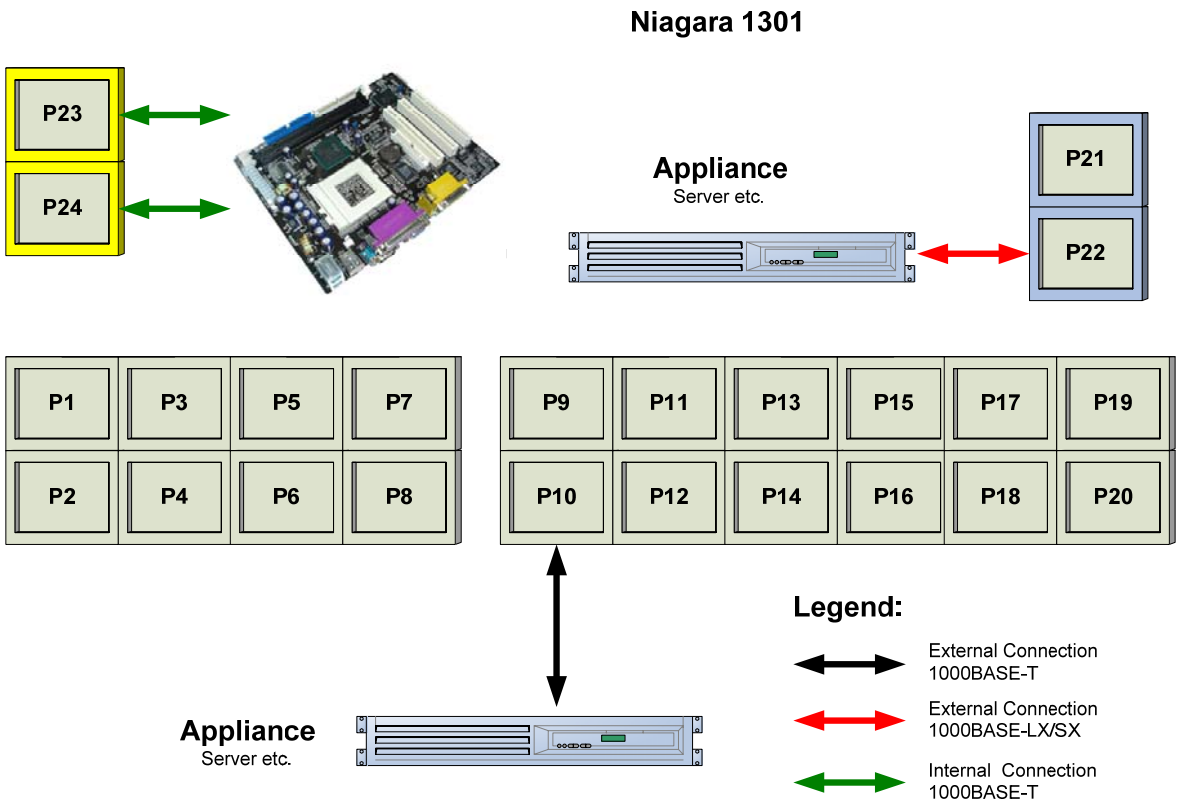

Figure 3, Niagara 1301 Diagram of Operation 1

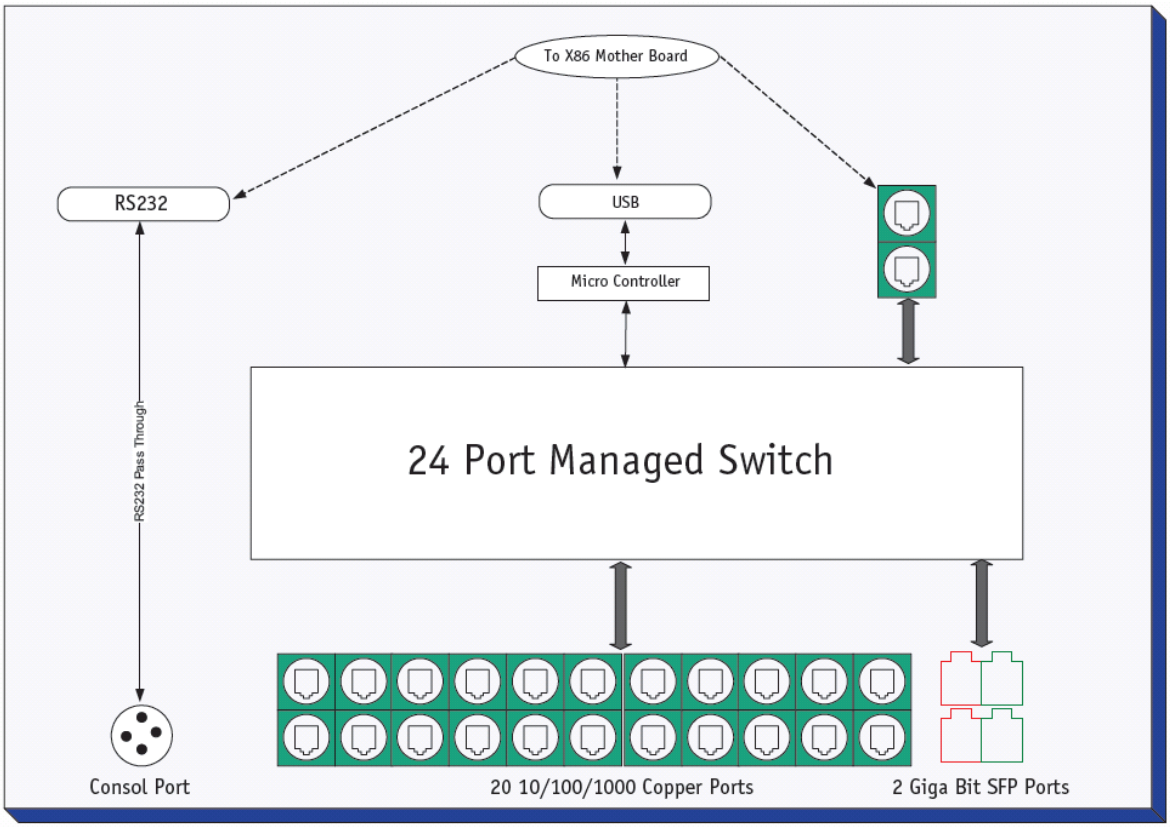

Figure 4, Niagara 1301 Diagram of Operation 2

2.2 USB Interface

Connector J3 is a USB interface, it is used to communicate between Niagara 1301 and the Motherboard. The user can run Utility commands under Linux or FreeBSD GUI to interact with Niagara 1301, eg, Firmware update, Register configuration.

The USB interface is getting power from the Motherboard through Pin1 of J3.

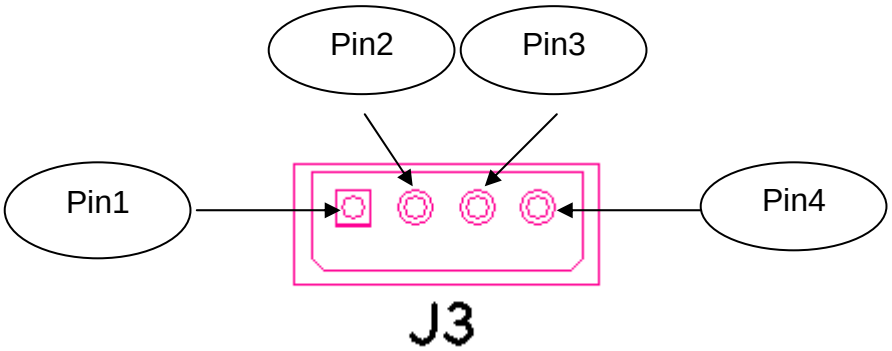

Figure 5, USB Interface

Pin1: +5V
Pin2: D-
Pin3: D+
Pin4: Ground

2.3 5V Power Supply Output

Connector J9 provide +5V power supply for the user.

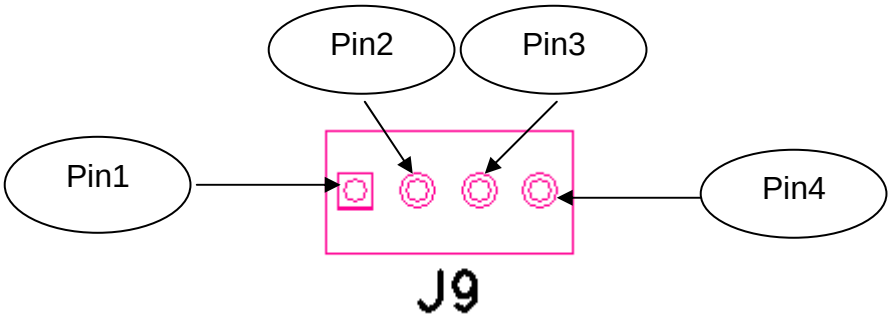

Figure 6, 5V Power Supply Output

Pin1: No connection
Pin2: Ground
Pin3: Ground
Pin4: +5V

2.4 Power Supply Input +5V and +3.3V

There are dual power supply input connectors (JP2 and JP3) on Niagara 1301, it provides the power input interface from the external power supply to Niagara 1301. +5V is come in through Pin2 and +3.3V is come in through Pin3.
Only one power input is needed for Niagara 1301 to work. The second power input should only be used when the external power supply can not provide enough current.

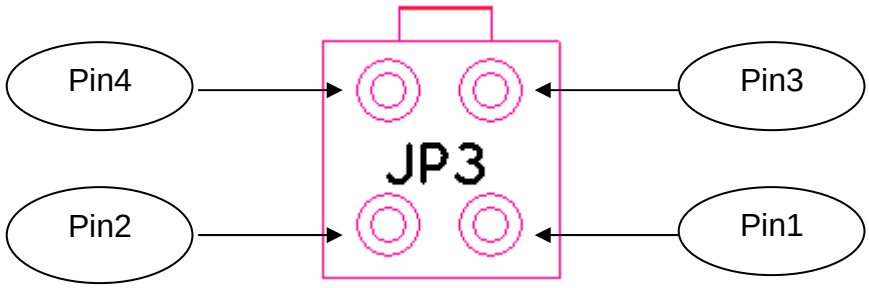

Figure 7, Power Supply Input

Pin1: +12V (Not Used)
Pin2: +5V
Pin3: +3.3V
Pin4: Ground

2.5 5V LED Panel Power Supply Output

Connector J8 is used to provide +5V to the LED panel. This output can be turn on or off by utility command.

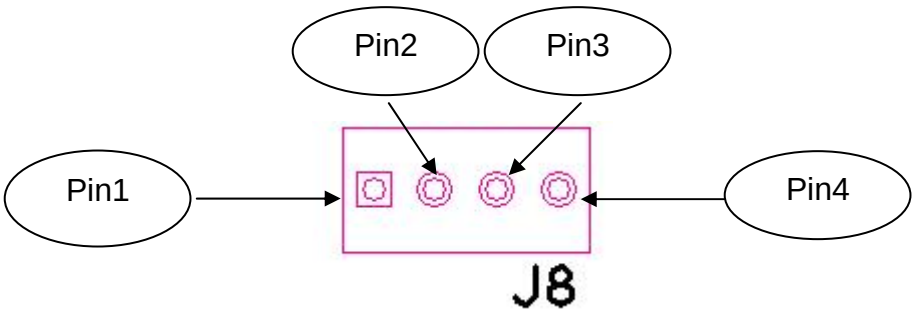

Figure 8, 5V LED Panel Power Supply Output

Pin1: No connection
Pin2: Ground
Pin3: Ground
Pin4: +5V Output to LED panel

2.6 Dip Switch

The Dip Switch SW6 is used to set different product ID for the user. For example, the user can set Dip2 and Dip1 both off to assign ID 70 for the system mode named IM1301A. The user can set Dip2 and Dip1 both on to assign ID73 for another system mode named IM1301D.

Figure 9, Dip Switch

Dip2	Dip1	Board	Product ID	System model
OFF	OFF	N1301	70	IM 1301 A
OFF	ON	N1301	71	IM 1301 B
ON	OFF	N1301	72	IM 1301 C
ON	ON	N1301	73	IM 1301 D

Table 2, Dip Switch Setting

2.7 Serial Console Interface

Connector J4 is used as Serial Console Interface input, connector J7 is used as Serial Console Interface output to the Motherboard. This serial connection bypasses through N1301 to provide interface for the user to interact with the motherboard.

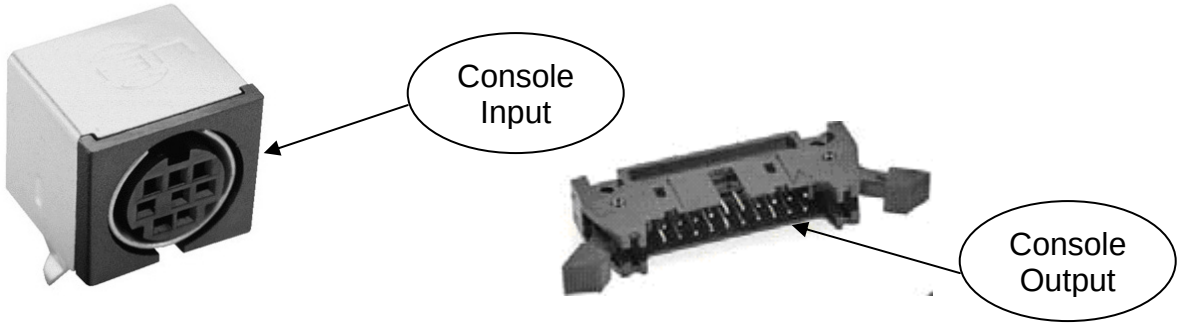

Figure 10, Console Interface

2.8 Copper Port LED Indicators

There are 2 LEDs Per Port that are visible from the front side of the boards.

Port Link LED

This LED turns on solid when there is link on port.

Port Activity LED

This LED blinks when there is any traffic going through port.

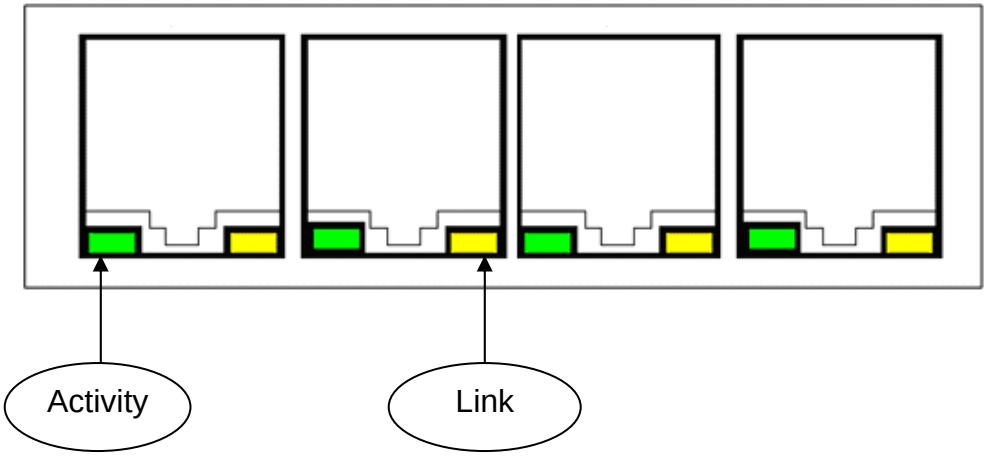

Figure 11, Copper Port LED Indicators

2.9 Fiber Port LED indicators

There are 2 green LEDs for each port to indicate the Link and Activity status.

Port Link LED

This LED turns on solid when there is link on port.

Port Activity LED

This LED blinks when there is any traffic going through port.

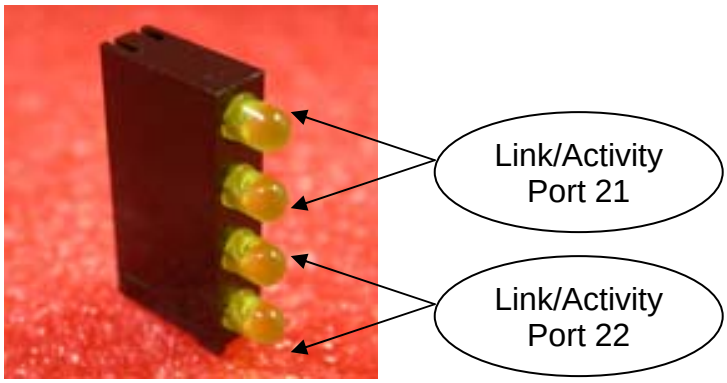

Figure 12, Fiber Port LED Indicators

3. Host Utility interface

Niagara 1301 has a USB Utility Interface for the user to interact with the control processor on the board. The user can run the utility commands to display the information of the board, indirectly configure the registers of Vitesse Switch and PHY, upgrade and verity the firmware.

3.1 Rebuild the command line host utility

To rebuild the utility simply type “make clean” and “make all”.

3.2 Stand alone host utility command line options.

The information of Niagara 1301 can be shown by the Utility commands show below:

To display help information,
```
“./cp300_util”
```

To display unit information,
```
“./cp300_util – n i”
```

To scan all unit,
```
“./cp300_util –c”
```

The LED panel can be turn on or off by the Utility command show below:

To turn on LED Panel,
```
“./cp300_util –C,l”
```

To turn off LED Panel,
```
“./cp300_util –C,L”
```

There are only 2 ports turned on after Niagara 1301 power up, P1 and P24. The rest of the Ports P2-P23 are called optional ports, they can be turn on or off by the Utility commands show below:

To turn on Optional ports,
```
“./cp300_util –C,p”
```

To turn off Optional ports,
```
“./cp300_util –C,P”
```

The user can access the internal registers through a serial of Utility commands. Before write/read the SW/PHY internal registers, the Firmware housekeeping needs to be stopped by command, "./cp300_util –S w,0".
Please see APPENDIX A for the example and APPENDIX B for port mapping.

To write firmware mode,
"./cp300_util –S w,<mode_in_hex>"
e.g "./cp300_util -S w,0" //switch firmware mode to 0

To read firmware mode,
"./cp300_util –S r"

To write to internal switch registers,
"./cp300_util –s w,<blk>,<sub>,<addr_in_hex>,<dword_in_hex>"
./
To read from internal switch registers,
"./cp300_util –s r,<blk>,<sub>,<addr_in_hex>"

Example:
./cp300_util -s r,7,0,0x18 //Read SW register "CHIPID"
//blk=7, block=7
//sub=0, subblock=0
//addr_in_hex=-0x18, register address=0x18

To write to internal PHY/external PHY registers,
"./cp300_util –p w,<ctl>,<phy>,<addr_in_hex>,<dword_in_hex>"

To read from internal PHY/external PHY registers,
"./cp300_util –p r,<ctl>,<phy>,<addr_in_hex>"

Example:
./cp300_util -p r,0,0,0 //read internal PHY register "PHY_CTRL"
//ctl=0, internal PHY
//phy =0, PHY address=0,
//addr_in_hex=0, Register address=0

./cp300_util -p r,1,0,0 //read external PHY register "Mode Control"
//ctl=1, external PHY
//phy =0, PHY address=0,
//addr_in_hex=0, Register address=0

To check link status,
"./cp300_util –p l,<port>"
e.g. ./cp300_util -p l,0 //check link status for Panel Port=1
e.g. ./cp300_util -p l,1 //check link status for Panel Port=2

To update Firmware,
"./cp300_util –U <*.bin>"

To verify Firmware,

```
"./cp300_util –V <*.bin>"
```

4. Document History

REVISION	ORIGINATOR	DATE EFFECTIVE	NATURE OF CHANGE
01	Kevin Yan	11/18/2008	Genesis
02	Kevin Yan	11/24/2008	Add examples

Table 3, Document History

Appendix A

Example how to access internal registers

```
1) Disable Firmware housekeeping loop.
./cp300_util -S w,0

2) Check to see switch housekeeping is stopped.
./cp300_util -S r
RD:Software mode = 0x0
firmware global tick/cnt = 0x81
Request timeout cnt LSB = 0x0
Request timeout cnt MSB = 0x0
Current House keeping loop port index = 0x0

3) Switch page register to GPIO page
./cp300_util -p w,1,4,0x1f,0x10
[PHY_WR] ctl 1 phy 4 offset 0x1f word 0x10

4) check to see we have switch the page
./cp300_util -p r,1,4,0x1f
0x10

5) Read back SIGDET register
./cp300_util -p r,1,4,0x0d
0xf
```

Appendix B

Ports Mapping

Port Index	Panel Port	SW Port	MAC BLOCK	MAC SUB BLOCK	PHY I/F 0 -Internal 1 -External	PHY ADDR	Connector	Type	PHY ADDR[4]	N1302 Config	N1301 Config
0	10	8	1	8	0	0	J5A	RJ45			
1	9	9	1	9	0	1	J5B	RJ45			
2	12	10	1	10	0	2	J5C	RJ45			
3	11	11	1	11	0	3	J5D	RJ45			
4	14	12	1	12	0	4	J5E	RJ45			
5	13	13	1	13	0	5	J5F	RJ45		12 xRJ45	
6	16	14	1	14	0	6	J5G	RJ45			
7	15	15	1	15	0	7	J5H	RJ45			
8	18	16	6	0	1	0x10	U12A -> J5I	RJ45	PHY ADDR [4] = 1		
9	17	17	6	1	1	0x11	U12A -> J5I	RJ45			
10	20	18	6	2	1	0x12	U12C -> J5K	RJ45			
11	19	19	6	3	1	0x13	U12D -> J5L	RJ45			All 22+2
12	22	20	6	4	1	0x14	U12E -> U7C	SFP			populate
13	21	21	6	5	1	0x15	U12F -> U7D	SFP			
14	24	22	6	6	1	0x16	U12G -> J6A	RJ45		2x RJ45	
15	23	23	6	7	1	0x17	U12H -> J6B	RJ45		to CPU	
16	6	0	1	0	1	0x04	U13E->J11E	RJ45	PHY ADDR [4] = 0		
17	5	1	1	1	1	0x05	U13F->J11F	RJ45			
18	8	2	1	2	1	0x06	U13G->J11G	RJ45			
19	7	3	1	3	1	0x07	U13H->J11H	RJ45			
20	2	4	1	4	1	0x00	U13A->J11A	RJ45			
21	1	5	1	5	1	0x01	U13B->J11B	RJ45			
22	4	6	1	6	1	0x02	U13C->J11C	RJ45			
23	3	7	1	7	1	0x03	U13D->J11D	RJ45			

Figure 13, Ports Mapping

Appendix C

Assembly Drawing

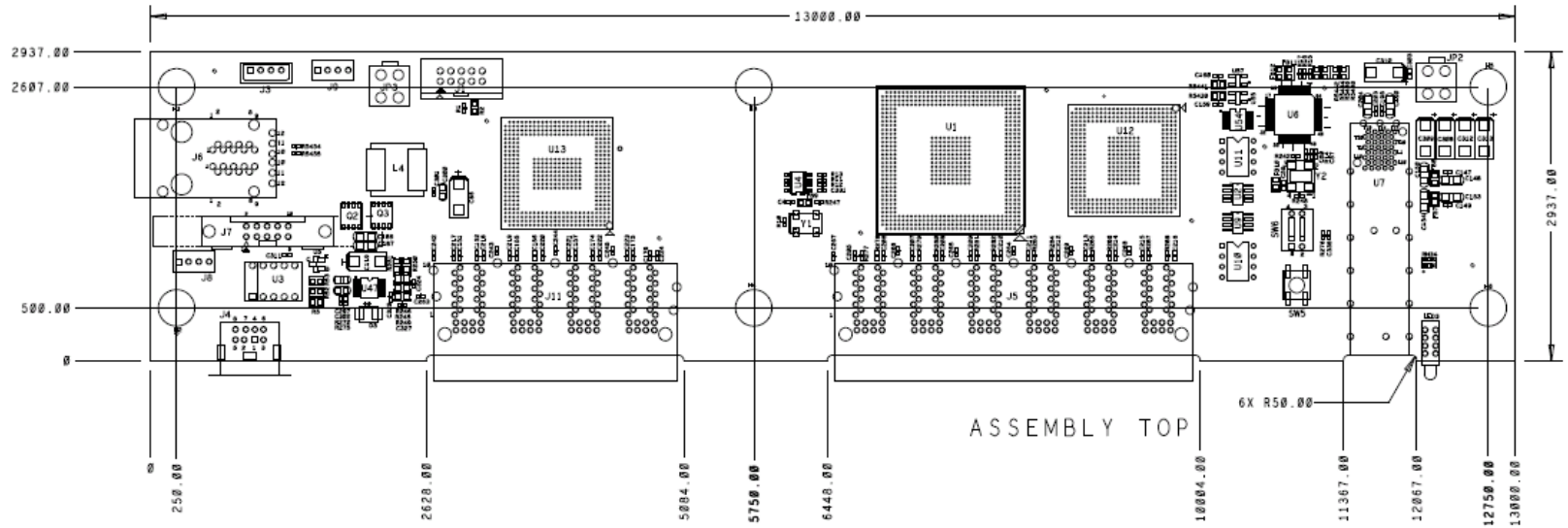

Figure 14, Assembly Drawing